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Process Predictive full-profile metrology

in the Semiconductor Market

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1. Summary

The potential of semiconductor process optimization for full-profile and film thickness metrology is not currently exploited in the market. Sales of optical digital profile metrology tools are occurring as a displacement of CD-SEM market share rather than through the use of their unique capabilities. This proposal discusses the current state of the market and potential product entry points for related segments involved in the semiconductor manufacturing cycle that involves the markets of device design, photomask manufacture and wafer fabrication.

The intention is not to restrict optical metrology participation to the historically defined market segments but to define a product philosophy that will encourage new, value-added additions to the market set for integration of both in-line and stand-alone metrology for full-profile modeling.

Two distinct needs in the industry are driving process predictive metrology:

1. The first market involves providing the proper toolsets for customer applications involving Advanced Process Control (APC) by a characterization of the lithographic feature shape or “profile” in anticipation of needs and drifts of the production sequence.
2. The second opportunity is a demonstrated need by the circuit designer employing reticle-enhancement structures, or “RET”s, for greater accuracy and end-process awareness during the semiconductor design sequence.

The APC market will require that continued measurements or “metrology” of each wafer batch be performed both inline to the production sequence, or on-board the lithography tool, as well as offline in stand-alone metrology tools. The need is epitomized by a requirement to go well beyond the simple gathering of data for statistical calculation that was the historic realm of metrology tools. The new applications will require data to be gathered that characterizes the full three-dimensional shape or “profile” of the imaged features on the wafer. The wealth of process information contained within these profiles can be modeled to extract the systematic variations in the process that are the source of yield and capacity limitation in the wafer production sequence.

Inline/onboard APC based process metrology satisfies the production need for rapid data gathering without bottlenecking of production flow. Sparsely gathered inline data would normally not contain sufficient information for an accurate determination of process drift or correction need. However when sparse inline data is convoluted into a series of perturbation signatures that characterize the lithography cell then a knowledge-based decision and correction can be calculated. Characterization data must be gathered offline and contains many more data points for analysis. However these signatures are static in nature and need to be re-calculated with a lower frequency than inline/onboard metrology.

Knowledge of the systematic variations present in the unique process of each customer during manufacture engenders the ability to apply these predictable causes back into the production sequence to stabilize and improve semiconductor yield. The concept of

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applying production models to wafer-metrology of test and production sequences in order to control and stabilize yields is called "Predictive Metrology". Only Weir PW software incorporates advanced models of this genre with the ability to successfully deconvolve the process control elements for the next generation of device designs.

The next sections will show how the proper collection of raw metrology data can be used to characterize the production response of a target customer wafer facility. The predictive models of Weir PW have the ability to convert this raw data into an understanding of the presence and magnitude of the controllable error sources within a specific customer wafer facility. A modeled characterization engenders an understanding of the base capabilities and error sources that contribute to the variations seen in product that directly influence yield. With specific knowledge of the presence and magnitude of these error sources:

- Optical Proximity Correction (OPC) elements on reticles can be tuned with greater effect and accuracy,
- Stability of the process can be maintained through the regular monitoring of specific control elements,
- New product or reticle introductions can be tuned to provide greater yields and faster product introductions
- New device-design process setup is more accurate than with classic methods because the variations encountered across the entire exposure field and with film variations is more precisely understood.

2. Overview

The classic approach to semiconductor process control has been to analyze metrology data using statistics and basic mathematics. Current semiconductor device designs do not support the wide process margins needed to assume the random data variations in production that are required by these statistics.

The design for manufacture (DFM) market has recently been dominated by a series of simulation products that that are used to calculate the proper feature size and structure on the photomask reticle. The reticle provides a single layer design of the device pattern and during production it is photographically imaged on the wafer. The DFM market is driven by the fact that reticle patterns that comprise each transistor or gate on the reticle and whose widths are near the resolution limits of the lens do not physically resemble the final structure imaged in the photoresist on the wafer. Software simulation of the lens-aberrated image is used to anticipate each reticle-design iteration by predicting the image that will appear on the wafer without having to expose and measure wafer structures.

Recent entries to the DFM market incorporate not only greater complexity but also specialty hardware. More significantly for our purposes, along with each new custom-designed hardware-core goes the grudging acknowledgment by these vendors that the simulation must be calibrated to the end-process of the customer using raw metrology. The simple calibration of the simulation currently performed involves the exposure and measurement of a series of test structures and is conducted as part of the initial setup for the customer. The response of these measurements to the process's natural variation provides the offsets and boundaries for future simulations for that specific customer.

Common to these two related emerging markets is a need for more metrology that includes a simple measurement of the width of each critical feature image in the photoresist of the wafer. In the real world, the image measured in the photoresist is not a simple two-dimensional artifact but a complex three-dimensional structure that is highly sensitive to production process variation.

Simple process metrology such as this that is conducted for one or two points in the exposure only approximate the true response interactions of the exposure tool, reticle and process. DFM calibrations incorporating the simple setup used are subject to soft metrology errors, localized variations in exposure and exposure tool perturbations that may differ significantly from those tested under the limited sampling involved.

The information contained within the wafer's 3-D profile structure has yet to be exploited in the market as a control element for improving yield. Only Weir PW software includes full-profile modeling capabilities that employ process-aware Predictive Models with the ability to deconvolve the contributors to process variation.

2.1 Metrology Trends

Historically, metrology in the semiconductor wafer fabrication facility ("Wafer Fab") has not been a value-added process step. The step is most often used for pass/fail determinations of product; the net result being that, at best, the current lot passes the metrology step without ill consequences. As a result there have been periods in the history of the industry when no metrology was performed during the entire lithography sequence.

These periods of operation without metrology correspond to those times during which process margins of the manufacturing tool set exceeded the demands of the device design rules. They have always followed the introduction of a new generation of exposure tool or lens design. Yet, as of the early years of this century, major leaps such as this have not occurred as the industry battles the physics of optics to reduce critical feature sizes below the wavelength of the actinic radiation.

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The market's unwillingness to invest in offline metrology is further clouded by the observation that some rejected wafers and lots, when subjected to additional measurement, will pass the statistical tests of the lot. Failures like this are the result of applying classic control statistics to sparsely sampled wafers.

Overlay Metrology Transitions

The sparse-data phenomenon was first recognized in the overlay metrology market in 1992.[1] The false predictions arise from the fact that errors in the semiconductor lithography are not distributed in a random format, as needed to be successfully described by classic statistics. Semiconductor errors are highly systematic in nature thereby exhibiting either highly concentrated or widely distributed populations. Sampling plans therefore will consistently under or overestimate the true distribution of lot errors when small sample sizes are taken.

The overlay metrology segment of the industry went through this stage in the mid-1990's. A viable manufacturing solution was found through the application of "machine models" that were developed from and whose coefficients corresponded to the adjustments needed to correct the systematic components of the overlay perturbations measured [2]. The models now provided an easy means of correcting overlay metrology and the need drove the KLA-Tencor as one of the first implementers of the technology into a predominant position in the market.

Model analysis however still required significant levels of sampling and could only be used as a feedback mechanism. A solution to the large sampling requirement was found by recognizing the stability of the perturbation signature for each exposure tool. Once derived, this "static" signature could then be combined with follow-up metrology patterns that gathered sparely sampled data from the product and combined their observations with signature to evaluate the current tool stability and accurately predict the overall modeled overlay performance for areas extending significantly beyond the sampled area [3]. As a result, wafers can be sparsely sampled and the results, when applied to the proper static model, can be extrapolated to accurately evaluate the true distribution of overlay across the lot during the determination of corrections and pass/fail gating.

The feature-profile metrology segment is now undergoing a transition similar to the overlay market of the mid-1990's. Unlike the overlay market, the driving forces are much stronger and yet to be exploited by any vendor.

Feature Profile Market Evolution

Two primary critical dimension (CD) technologies contend for direct production support; the automated Critical Dimension – Scanning Electron Microscope (CD-SEM) and visible light, optics based tools using a technology that we shall refer to as Optical Digital Profilometry (ODP). Other profile capable technologies exist but are either too slow or they require electrical connectivity for measurement. These other technologies are thus relegated to the much smaller markets associated with equipment and process setup.

CD-SEMs have been a workhorse in the Wafer Fab for over a decade and are well known commodities. Their problems arise in the tradeoffs between precision, speed and damage to the area under test. Precision and speed dictate a high-voltage potential acceleration of the electron stream. However this high current flux in itself leads to carbonization and localized charging of the substrate. When charging occurs the measurement error increases and the wafer surface is contaminated with hydrocarbons.

Two companies have viable, profile-capable CD-SEMs; KLA-Tencore and AMAT. The AMAT and KLA-Tencore CD-SEMs generate the 3D profile of the feature using specimen tilt and/or detector positioning. These CD-SEMs can output profile height, width and slope as well as edge-roughness. The unique offering of the SEM over the ODP approach is its ability to measure the foot of the profile and line-edge roughness. The SEM exhibits several shortcomings for a production tool in addition to the high level of maintenance such as the need to move the wafer into a vacuum and the charging and deposition of material on the wafer surface. An even more sinister problem recognized by advanced users of modeling is the frequency of soft errors present in the raw data. Soft errors in metrology result from improperly captured target locations and the small area of measurement on the feature. They are present in all metrology data but their occurrence is greater in the CD-SEM.

The ODP approach uses a full nested area of features. Dense packed features can be measured with like accuracy to "isolated" features when the period of feature placement in the target exceeds three-times the feature size. While OPD averaging still occurs over a small area of the chip that is usually 50 um in size, the SEM scans an individual feature edge of a feature covering an area of only a few nanometers or at most a micron. . The averaging of a number of linewidths is an advantage for APC and Predictive

[1] T. Zavecz, "Lithographic overlay measurement precision and calibration and their effect on pattern registration optimization", Proc. SPIE vol. 1673 (1992), p. 191-202

[2] T. E. Zavecz,"Machine Models and Registration", SPIE, CR52-10 (1993).

[3] T. Zavecz, R. Blanquies, "Predictive process control for sub-0.2 um lithography", Proc. SPIE vol. 3998_48 (2000)

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Metrology. Process control relies on the averaged response of the image and not the variations that an SEM sees within the few molecules of the structure scanned by the SEM.

ODP tools incorporate either ellipsometer or scatter analysis and wavefront-scatter or “RCWT” models to reconstruct the feature profiles. These tools have an added benefit of providing the full-feature profile as well as the thickness of all translucent films in the device surface.

The defining characteristic of the CD-SEM is found in the small sample area and ability of the technology to measure a single site precisely. This characteristic is viewed as a shortcoming when the averaging needed for process and tool characterizations is desired therefore requiring larger sample sizes to be taken by the SEM that average over the local variations of the film stack and surface influence.

ODP tools on the other hand can quickly take full-profile and film data from an area that removes localized effects of the substrate. The ODP measurement target is relatively large and requires an area on the device to support a 50 micron target grating. The ODP tools, unlike the CD-SEM, can be physically contained within very compact footprint and lend themselves will to multi-function stand-alone stations or to Inline Metrology (IM) modules capable of mounting directly on a clean-track of the exposure cell.

All of the ODP tool competitors have been addressing the battle of focusing on a market consisting of a replacement of the CD-SEM. Similarly, no market-model appears to properly address the differentiation between stand-alone and clean-track formats. The greatest advantage enjoyed by the ODP technology, the full-profile and film-thickness metrological capability, is ignored but for a few specialized engineering studies. ODP tool market penetration is therefore currently nothing more than CD-SEM displacement.

Predictive Metrology can be used with either CD-SEM or ODP data. A characteristic common to any model is the fact that the more process information taken with each measurement, the greater will be the models ability to understand the contributors to deformation. Data collected by ODP tools therefore provide a greater potential for both control optimization in the process. The need for Predictive Metrology is driven by:

- the ever-shrinking process margins that characterize progress in this industry,
- a further reduction in the random-error components of the semiconductor process,
- an increase in the significance of the systematic, and therefore controllable, process fluctuations that directly result in yield loss and
- the necessity to anticipate feature response for process corrections that enable short-loop feed forward and feed back control loops.

These needs present themselves in both the Wafer Fab and Mask Manufacturing components of the industry.

The DFM Market need for Predictive Metrology

A less well recognized opportunity lies in the Design for Manufacture market. This is a young market in which companies such as Brion and KLA-Tencor offer hardware based, enhanced simulation tools for feature design. These markets are driven by the need to properly simulate feature designs on photomask reticles incorporating Optical Proximity Correction (OPC) based structures. OPC structures are active lens elements on the reticle that allow the exposure tool to properly image features smaller than the wavelength of the light used in the imaging sequence. This imaging trick is achieved by having the critical feature actively modify the wavefront in its locality using advanced techniques such as localized phase-shifting of adjacent image-rays or controlled scattering to interfere and enhance the final image on the wafer. These masks are expensive because of the additional etch and alignment steps required for their construction.

DFM simulators start with a reticle design and then introduce lens aberrations to determine the shape and characteristics of the final wafer image. Unlike classic simulations such as employed in Prolith from KLA-Tencor, these offerings contain hard-coded hardware in a custom-designed computer to calculate the images. Unlike Prolith, the speed of the hardware-based simulators allows many critical elements on the exposure field to be simultaneously calculated for improved accuracy and scope. Also unlike Prolith, for the first time it is now very important for these simulators to be “calibrated” to the target wafer process.

The calibration consists of a simplified process window calculation from basic feature-width metrology to set the proper variables for focus, dose and size of the process window. One of the offerings will soon be adding in a simplified set of customer-specific lens aberrations to generically calibrate to the type of exposure tool used in the target customer facility. In summary, these simulators are used in the final design of the photomask to optimize the phase and scatter-bar construction shapes of the OPC structures on the reticle.

An adjunct technology called “Inverse Lithography” has been introduced by Luminescent Technologies. Luminescent again uses a hardware-accelerated simulation tool but now the final image on the wafer is the starting point. Quite naturally, this final image looks like the chip-design structure for the integrated circuit. The Inverse Lithography analysis then introduces a set of optical

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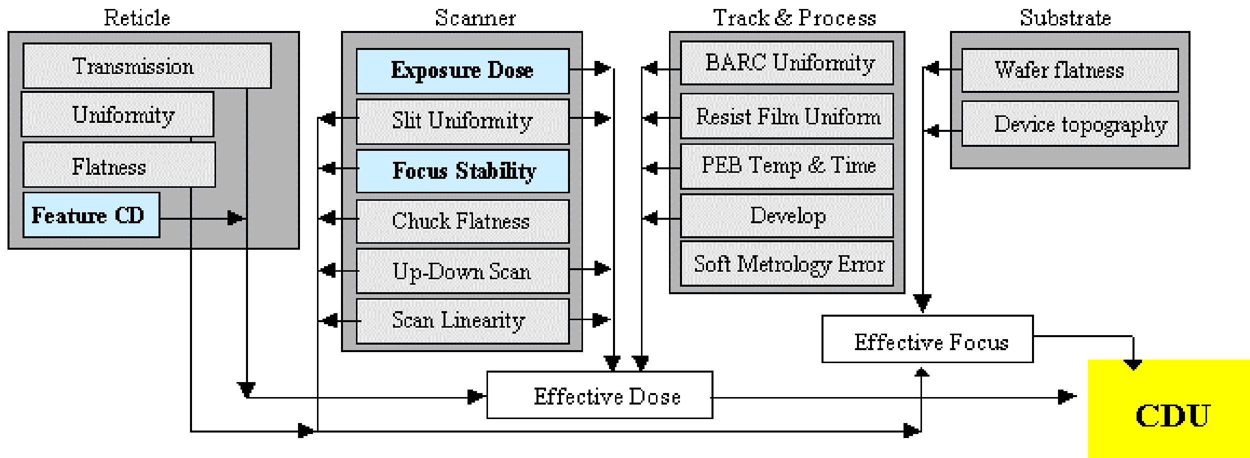

Figure 1: Perturbation sources of Critical Dimension Uniformity (CDU)

aberrations to inversely calculate a binary image on the photomask. Unlike classic OPC structures, the photomask does not require additional etching and alignment steps in its manufacture. However these new reticle-designs do not generate the easily produced rectangular shapes generated by most photomask production tools but can contain many feature elements of any size, shape and orientation. The mask sets therefore are very complex and expensive.

The two advanced OPC tools just described are "calibrated" to a focus-dose matrix of critical linewidths that is measured and passed into a process window calculation. The metrology and analyses are basic and easily performed with today's equipment. This simulation technology however is in its infancy and is focused on product in the 90 nm node and above. These calibration techniques will not provide the accuracy needed to support the next generation of device.

The images generated during semiconductor production contain four major sources of systematic error shown in figure 1. These four sources contribute a total of seventeen systematic signatures that can be tuned and controlled to optimize a photolithography cell during manufacturing. Of these seventeen variables, the OPC simulators today consider only two; focus and dose. The remaining variables introduce significant errors into the simulation that will become more and more significant as these products mature and the industry drops to device nodes of 45 nm and smaller feature size.

This is an opportunity for the rapid, profile measurement of ODP combined with the adaptive and predictive models of Weir PW to provide significant yield improvement to the semiconductor industry.. The Predictive Metrology models developed by TEA SYSTEMS CORPORATION can perform the needed deconvolution of these error sources. Once identified, each error source can potentially be used in the DFM sequence to correct and optimize the simulation with greater accuracy than a simple process window calculation. The accuracy and stability of the calculated corrections is enhanced by the adaptive nature of the TEA System's proprietary models as well as their ability to incorporate the full metrology gathered from ODP wafer metrology

The industry is moving in a direction that will soon need to optimize critical mask layers for the specific end-user production facility. They will also need the ability to gather full-profile data for the calibration of these simulators and optimally combine photomask-gathered structure data to enhance the discrimination of wafer-process induced variations from those introduced during reticle productions.

The next section discusses these opportunities in greater detail.

3. Market Opportunities of ODP Predictive Metrology and TEA Systems

Aerial image simulations, such as Prolith, currently predominate both the Photomask and Wafer Fab markets for process setup and design verification. Most approaches are not firmly calibrated to process response and therefore only approximate the behavior of the system over a small and idealized region of the exposure field. Exceptions to this are now arising in offerings from Brion and KLA-Tencor.

Advanced Process Control (APC) loops have failed as generic products in the market with the exception of a few simplified applications such as those offered by Brooks Automation. Wafer production facilities have for the most part taken on the task as part of their internal factor control efforts with varying degrees of success.

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Short-loop APC functions, within a single tool, have been successful in ASML and AMAT. Short loops between tools, such as a Clean-Trac to ASML scanner interface have yet to be realized however the manufacturers are installing the software portals needed for this control.

The most immediate application opportunities reside in a path that parallels the overlay market of the past decade. Empirical data gathered and modeled using full-profile aware film and machine models will provide both enhanced short loop process controls and advanced lot gating during production. Simultaneously the customer will enjoy the real time benefits of tracking the systematic trends of the process and tool set to schedule maintenance and tuning in a controlled environment through the use of Predictive Modeling.

Implementation will vary by process sector and is addressed in each in the following section.

3.1 Device Design Segment

Companies such as Synopsys and Cadence use simulators for chip design to optimize device electrical response. Recently driven by Design for Manufacturing (DFM) pressures, the design segment has recognized the importance of including reticle enhancements (RET), such as Optical Proximity Correction, in the design phase of the device. Previously this chore was left to the mask-manufacturing segment.

Chip designs that employ RET constructions often require hundreds of hours of data preparation computation prior to the exposure of the photomask. RET behavior is not intuitive and implementing designs directly onto the photomask without validation is costly in both time and money. Design segment companies therefore need to implement device validation techniques using wavefront simulations that take into consideration the sub-wavelength behavior of the circuit elements. Existing techniques implemented by software such as Prolith and Sigma-C are simplified analyses and are regulated to small parts of the device field. These packages employ little or no calibration to actual process results and their results therefore approximate the response over a very small fraction of the chip. Expanding the application of these software tools to full-chip designs is both time-prohibitive and violates the design base of the software. The industry is therefore turning to new implementations.

KLA Tencor's DesignScan simulator addresses the long simulation times using an integrated software system on high-speed computers. Even more aggressively, Brion formally entered the industry in February 2005 with a custom designed hardware-accelerated modeling package intended to speed up this simulation chore. Unlike the KLA competitor, Brion calibrates their simulation to five points in the focus-dose exposure window. This calibration was the focal point of the company's marketing presentation at BACUS 2005 and represents an improved method of instilling process-traceable response for reticle OPC feature optimization that will function over the range of normal process variations. There exists no method of validating the full-field results of these calculations and the benefits of predictive profile modeling are neglected..

PDF Solutions and some university offerings implement proprietary electrical test structures to calculate OPC design rules prior to committing a device and it's RET features to photomask generation. This early implementation of the design optimization provides faster ramp-up of new designs that are customized to the process and tool set of the chip manufacturer. PDF does not validate the optimizations during manufacturing and relies solely upon probe-yield results for confirmation. Many of their electrical structures could be employed as profile-based metrology gratings thereby shortening the test time and the need for multi-layered metallization.

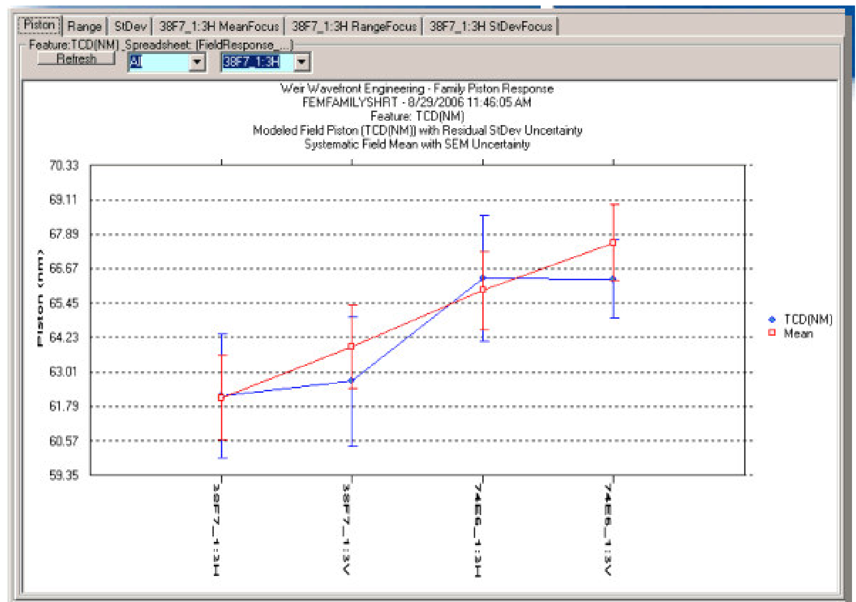

Figure 2: OPC evaluation for 65 nm, 1:3 Vertical & Horizontal features; a comparison of two specific design choices derived from full-process variations.

All techniques described neglect the benefits that could be derived from a calibration of their reticle-structure design simulators to the exposure-tool perturbations engendered by variations in dose, scan, coherence and aperture across the exposure field. These are the major source of variation within the process and their inclusion and feedback to the device designers can add a level of design for manufacturing (DFM) enhancement not currently envisioned.

Product offerings in this segment derived from ODP measured profiles using Weir PW can be

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used to validate the full-chip response of all reticle enhancement constructs. Unlike present techniques, device response beyond the simple theoretical process window can be extrapolated to include the customer's unique toolset and process perturbations. Results are then fed back to the device designers for additional optimization in subsequent photomask versions and for improved calibration of their simulators.

Weir PW's OPC extraction software allows the full profile fluctuations unique to the customers wafer process to be accurately broken down into systematic and random error sources as shown in figure 2. Figure 2 shows both the difference in feature size derived from two strategically different OPC designs and their response to lens-slit scan averaging of the feature. Systematic error segments are further deconvolved to assign their origins to portions of the process, scan, lens, reticle and mechanical segments of the image generation steps. The true, full-exposure-field response of the OPC or RET design is therefore accurately evaluated not only for base performance but also for robustness to daily process fluctuation and tolerance to tool excursions. Even small differences in OPC design structure can be noticed using this method and incorporated into a reticle design optimized for the end-process of the customer facility.

3.2 Photomask Segment

Historically the photomask industry has relied upon metrology sampling for simple production gating. Concepts involving full-plate modeling of metrology data and spatial sensitivity to perturbation sources are not implemented in this segment. There is very little linkage of reticle manufacture perturbations with those noted in the wafer fabrication facility.

Reticle enhancements are a constant and recognized problem for this segment. Feature perturbations in Optical Proximity Control (OPC) based features can result in photomasks that fail when subjected to the stresses of the customer's full process window or through repeated use and subjugation to production exposure of actinic radiation. Phase shift mask problems have raised the mask-maker's awareness of the critical nature of chrome and chrome etch profiles. A significant number of papers at the BACUS 2005 conference were dedicated to the recognition that phase shifts are not optimized at the theoretical wavelength etch depths but must be tuned to the chip design. Inherent in this is the need further optimize these etch depths to the unique characteristics of the wafer-fab customer's process and the influence of the film uniformity and toolset inherent within it.

The models of Weir PW software applied to photomask reticle data provides added benefit in all these areas of the photomask segment. OPC corrections directly measured on a reticle through grid constructs are spatially modeled for uniformity by the software. The results of these models provide critical film and profile signatures to the photomask segment that can improve uniformity. These signatures obtained for a specific reticle can be resold to the semiconductor segment customers as a valuable part of a reticle signature library. Users of Weir PW in the semiconductor wafer fab then use these library entries for in-process validation of the reticle quality and rapid setup of new processes.

Phase shift technology (PSM) masks also benefit from the use of predictive metrology to validate etch depth as well as film and feature profile spatial uniformity. Since the actual etch depth must be tuned to the periodic structure spectrum of the photomask, Weir PW models provide a natural solution for calculation of etch optimizations.

Binary mask chrome edge quality is a critical factor in determining the lifetime of the photomask. Undercut edges will result in exposure flare during use and the physical structures will eventually fail as a source of daily use in wafer production.

Normal production gating in the photomask segment can be improved using the data modeling of Weir PW. Implementation of the Weir PW product is used to improve the poor quality estimates resulting from statistical sampling. Unlike classic sampling, Weir PW does not assume the data to be random. Systematic variations when modeled can be accurately predicted across the entire reticle. Reticle process gating based on these predictive modeling techniques not only increase yield but every reticle measured acts as a test vehicle to monitor the continued quality of the production sequence.

The cost of the system to the photomask segment is offset by their ability to provide additional products to their customers in the form of profile and film uniformity maps and feed-forward enabling reticle signatures.

3.3 Semiconductor Production Segment

Many segment customers including Sematech's immersion team believe that the advantages of the Optical Digital Profilometry (ODP) will disappear below the 45 nm node because of the technical constraints of thin film ellipsometry.

The current state of critical feature metrology in this segment is similar to that experienced by the overlay market prior to the implementation of model-driven process optimization and tool tuning. An awareness of the need for full-wafer and exposure-field tuning is arising within the internal tool qualifications run by ASML. ASML is driven by the complexity of the electo-mechanical and optical interactions of their product line. Initial implementations therefore need to model uniformity across the lens slit, exposure field and the entire wafer.

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ODP full profile metrology, enhanced through Weir PW modeling, provides much more than exposure tool corrections and perturbation analysis. The full-profile interactions of film and design gratings on production wafers are analyzed to provide the customer with a real-time monitor of the most critical variations in the process influencing device yield and performance speed.

Semiconductor International's September 2005 issue provided an overview of Advanced Metrology in the industry. KLA-Tencor expressed the recognition of hidden systematic errors in the process that can be modeled and corrected using only the full-profile capabilities of ODP technology. The focus of KLA however is myopically constrained to full-lot sparse data sampling as dictated by the historic methods of CD-SEM methodologies. Wafer-to-wafer variations however are not the greatest source of perturbations in the industry but they are the most successfully addressed problems that can be detected by the sparse sampling inherent in in-line metrology (IM).

Predictive Metrology model development is cited as a needed enhancement for the segment but is constrained by the lack of a good solution for reliable result prediction using sparse data samples. This is an unfulfilled niche in the market that will provide both technological and intellectual barriers to entry for Weir PW Predictive Metrology competitors.

Timbre currently offers a process window software option on their PAS computer. This option automates data gathering and analysis using classic Monolith and Prolith techniques for process window analysis. There is a need in the industry for this type of analysis however the Timbre and other offerings do not favor full-profile metrology nor do they address the variations of the full-field exposure.

Weir PW provides automated classic process window analysis extrapolated to performance metrics across the full exposure filed. Additional features of full-field visualization of the window and its response to focus and scan perturbations can be offered to the customer. These features, implemented for full-profile and film response, are unique to the Weir QPC product and will carry the product market beyond the constraints of CD-SEM displacement.

Sub-90 nm node fabrication techniques on 300 mm substrates are moving toward single-wafer processing. Single wafer processing must implement short control loops of feedback and feed-forward information. Static process signatures derived from sparse in-line OCP data samples and Weir PW can be convolved with dynamic process perturbation signatures developed off-line. These signatures collected prior to exposure can then be fed forward to the exposure tool to optimize focus and dose corrections based on film thickness uniformity models.

Post-exposure IM measurements of film uniformity is another component that provides feed-forward information for develop and PEB optimization. The IM measurements after develop generate feed-back to the system as well as a perturbation based analysis of the health of the exposure system.

The value of the offline analysis is enhanced through the reticle signatures obtained from full-feature measurement of the reticle. The analysis is used to remove the reticle errors from any process setup or change to obtain a clear view of the process reaction. This information forms the basis for assigning the majority of the sources of the Mask Error Factor to hard corrections. Proper identification of these error sources and their magnitude allows them to be used to properly tune the reticle, exposure tool and films sequences of the production cycle.

Dose and Haze monitors on product

Ammonium sulfate ((NH4)2SO4) deposits on both the projection optics of the exposure tool and on photomask reticles are an increasing problem in the industry. They arise from the production process used in photomask manufacture and, for the case of hydrocarbons, the initial chemical reaction that occurs during photoresist exposure. These deposits are typically described as "haze". Their buildup on the surface is gradual and results in the slow deposition of an energy absorbing film. Haze slowly creeps into the process, gradually increasing the required exposure-dose over time. A production facility therefore finds production output slowing down to lower and lower levels.

Capacity loss is not the most critical result of haze build-up. The haze itself deposits unequally over the optical components. Exposures directly experience a gradual degradation of the process window, device yields slowly drop and rework rates increase. Also during this process the optical integrity of the image degrades. Scatter and flare increase within the exposure tool, aberration characteristics of the lens change and the effective dose received by each exposure field drastically changes particularly at the field edges. Overall the lithography cell experiences a reduction of control for processed critical features, feature profiles change continuously and an increased level of early device failures in packaged and shipped product soon follows.

Weir PW provides the ability to map dose and focus uniformity across the exposure field for any product. This means that any production layer can be used as a test reticle to confirm process window, depth of focus, exposure latitude as well as contour maps of effective dose uniformity and focus. Hand in hand with this capability is the Weir MACRO features of the Weir product line that allow these analyses to be fully automated in the Weir DM and DMA product line. Since Weir DM includes a long term trend charting capability, the onset of optical haze can be early detected, monitored and tracked to schedule optimum time for process maintenance.

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4. Predictive Modeling- Requirements

Simple spreadsheet models cannot be successfully used in the deconvolution of the many sources of variability in the semiconductor process. The design of the model, it's elements and the constructs used to gather, prepare and segment the data must be highly aware of the process sequence and the interactive nature of every process tool and film.

State of the art for process setup continues to follow the basic model for photoresist interactions first presented by John Bossung in 1977. This is a simplified interaction concept that has had several thousand papers reference it over the years and no significant improvements have been implemented since. It is inconceivable that an algorithm constructed for the technology of that era and not referencing the basic physics of the process could still be relied upon as the major control in today's technology.

Wide selections of process window tools are available today. They are all based upon Bossung's original work and differ only in the manner of their regression. Their major drawback is that they are nothing more than a polynomial expansion used to explain the predominant observations of focus and dose on a feature width. Their use is highly subjective and results vary significantly with the location of the measurement on the profile and the profiles location in the exposure field. The process window method begins to break down when more than one feature type is examined. The results obtained grow even more obtuse when trying to work with the variations seen for multiple points across an exposure field due to the cross interactions of lens aberrations and the process film stack.

The most critical photolithographic task involved in the introduction of a new semiconductor device is the final design tweak of the structures on the reticle for OPC structures. Many unsuccessful attempts have been made to use the process-window analysis for this task.

Predictive Models for feature profiles include an awareness of their construction sequence and the artifacts of variability of each tool used in the construction. The final feature profile is a convolution of perturbations added to the reticle feature from many sources. In the terminology typically used by mathematical approaches to control systems the process window approach is a global model that attempts to explain a complex variation using a simple end-point model of observations. In the complexity involved in the full feature profile an algorithm must learn and adapt to the observed data. High accuracy is not possible without a clear methodology and some prior information about the data and the process steps.

These algorithms must therefore be based on the specifics of the process contributors by applying models that enforce a multiplayer perception of the sources of perturbation and a scaled vector regression for extraction of the local signature.

A model handling these requirements must:

- be designed to be aware of the relative magnitude and range over which the source errors are introduced,
- be able to automatically extract sites where poor metrology is introduced,
- follow a multi-level sequence of analysis that allows the systematic perturbations of one source to be extracted from the data before passing it on to the next step,
- reflect the correctable sources of systematic error and not simply fit an algorithm to the data,
- adapt to variations in the number of data points and their locations on the wafer, field and sub-field elements,
- automatically extract and ignore singularities in the data and
- adapt the model elements included in the analysis to the significant perturbations present in the data sample,
- ignore sources of error not present in the data.

5. Conclusions

Recent years have seen a reduction in the use of off-line metrology in the semiconductor production cycle. In-line metrology taken during the production sequence has increased moderately with the objective of providing rapid statistical calculation for product gating and, in a few cases, feedback to correct for process drift. Increased use of process simulators have served to provide the predictive information needed to anticipate the final image quality from advanced techniques involved in reticle enhancement.

Metrology data has historically been employed with statistical tools to implement both product gating and to control stability. Statistical methods do not cope well with the systematic perturbations of a tightly held process. Corrections employed under these conditions soon involve over estimation of the perturbation that either results in a uncontrollable ringing of the process or the engineers under-utilization of each update that dampens response and limits yield improvement.

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The effect of these technical realities has been to reduce or limit the implementation of extensive metrology during production. This in turn has narrowed the range of metrology vendors in the market.

Changes to this trend are foreshadowed by recognition within the Design for Manufacture segments of the market now express a need to calibrate simulators to more accurately meet the anticipated performance of the customer production facility. The needs of the DFM segment precede those experienced in the Photomask and Wafer Process segments.

Coupled with the need for improved simulator calibration is a rising awareness in the semiconductor process of the increased significance of systematic, and therefore correctable, fluctuations within the production cycle. Metrology models capable of not only determining the current state of the process must also incorporate features that allow the sources of variation to be deconvolved as control elements for production.

Deconvolution is complex. The models employed require a strong knowledge of the process interactions as well as the ability to adapt to the characteristics of the metrology data gathered. Weir PW Predictive Metrology models provide this capability.

Weir PW models are capable of extracting the calibrations needed for proper calibration of DFM simulation software. The data gathered during this phase of the project can also be used as part of the photomask reticle manufacturing process in tuning the OPC process to the needs of the specific customer facility.

Photomask measurements employed in Predictive Metrology are valued both as process control features for the mask facility and as a valued characterization of the OPC Reticle as it is employed within the semiconductor process.

Semiconductor process setup is required for each new device design and periodically with each new change in process chemicals. Process setup that employs the information of the perturbations introduced by the reticle can determine with greater accuracy the response of wafer production to tool and process variations. Better setup interprets directly into improved device yields.

Process stability can also benefit through the use of full-feature profile metrology in the feed-forward elements of the APC environment. Process fluctuations are first noticed in changes in the resist profile and then later in the width of any given feature. Predictive Metrology Models incorporate these profile changes into a empirically derived control element. The power of Predictive Metrology is realized in the ability to accurately prophesize the response to process corrections and to determine extended performance of the elements under situations where data collection is sparse.

Predictive Metrology models that employ a full-profile knowledge of the process fluctuations will soon form the basic control elements to the extended markets of semiconductor device fabrication. Those facilities first employing these elements will in turn be the first to reap the profits obtained form a rapid, high yield introduction of each new semiconductor device into the market.

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